ABSTRACT:

Three-dimensional (3D) integration, a breakthrough technology to achieve “More Moore and More Than Moore,” provides numerous benefits, e.g., higher performance, lower power consumption, and higher bandwidth, by utilizing vertical interconnects and die/wafer stacking. Advances in 3D integration enable us to design radically new on-chip interconnection fabrics that can support exascale computing by integrating a very large number of embedded cores. Existing 3D Network-on-Chip (NoC) architectures predominantly follow straightforward extension of regular 2D NoCs.

However, this does not exploit the advantages provided by the 3D integration technology appropriately. In this context, design of small-world network-based NoC architectures is a notable example. We will show in this presentation how this concept of small-worldness can be adopted in 3D NoCs. More specifically, the vertical links in 3D NoC enable the design of long-range shortcuts necessary for a small-world network. These vertical connections give rise to the concept of physically far but logically near links while implementing the shortcuts. We will explain how machine learning can be leveraged to
intelligently explore the design space to optimize the placement of both planar and vertical communication links for energy and thermal efficiency.

**BIO:**

Partha Pratim Pande is a Professor and holder of the Boeing Centennial Chair in computer engineering at the school of Electrical Engineering and Computer Science, Washington State University, Pullman, USA. He is currently the director of the school. His current research interests are novel interconnect architectures for manycore chips, on-chip wireless communication networks, and hardware accelerators for biocomputing. Dr. Pande currently serves as the Editor-in-Chief (EIC) of IEEE Transactions on Multi-Scale Computing Systems (TMSCS) and Associate Editor-in-Chief (A-EIC) of IEEE Design and Test (D&T). He is on the editorial boards of IEEE Transactions on VLSI (TVLSI), ACM Journal of Emerging Technologies in Computing Systems (JETC). He was the technical program committee chair of IEEE/ACM Network-on-Chip Symposium 2015. He also serves in the program committee of many reputed international conferences. He has won the NSF CAREER award in 2009. He is the winner of the Anjan Bose outstanding researcher award from the college of engineering, Washington State University in 2013.

**For more information, call the EECE department office at (414) 288-6820**

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